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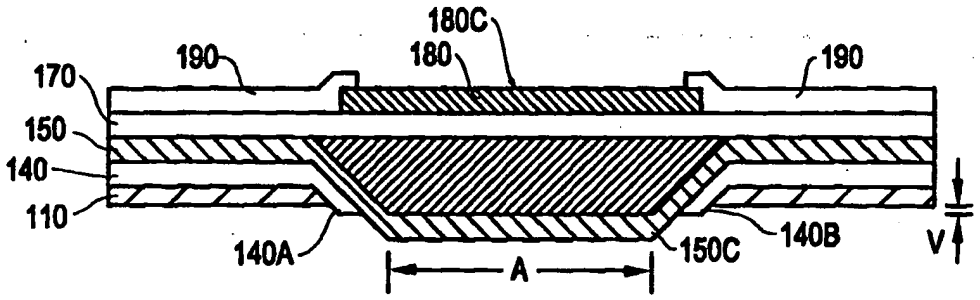

(57) Abstract

To fabricate back side contact pads that are suitable for use in a vertical integrated circuit, vias are made in the face side of a wafer (110), and dielectric (140) and contact pad metal (150) are deposited into the vias. Then the wafer back side is etched until the metal is exposed (150C). When the etch exposes the insulator at the via bottoms (140A, 140B), the insulator is etched slower than the wafer material (e.g. silicon). Therefor, when the dielectric is etched off and the metal is exposed, the dielectric protrudes down from the wafer back side around the exposed metal contact pads, by about 8 μm in some embodiments. The protruding dielectric portion improve insulation between the wafer and the contact pads when the contact pads are soldered to an underlying circuit.

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INTEGRATED CIRCUITS AND METHODS FOR THEIR FABRICATION

BACKGROUND OF THE INVENTION

The present invention relates to integrated circuits, and more particularly to chip interconnection and to forming contact pads on the back side of a semiconductor chip, and also to thinning of integrated circuits after circuit elements have been fabricated.

Some techniques for forming contacts on the chip "second" side are disclosed in U.S. Patent No. 5,270,261 issued December 14, 1993 to Bertin et al. and entitled "Three Dimensional Multichip Package Methods of Fabrication". Alternative techniques are desired.

SUMMARY

The invention provides methods for making back-side contact pads in a semiconductor die (or "chip"). The back-side contact pads are suitable for connecting the die to an underlying die to form a multi-die vertical integrated circuit. The invention also provides vertical integrated circuits. In addition, the invention provides methods for thinning of individual dice whether or not the dice will be part of a vertical integrated circuit.

In some embodiments of the present invention, back-side contact pads are formed as follows. A masked etch of the face side of a semiconductor wafer creates a via over each location where a back-side contact pad

is to be formed. A dielectric is deposited over the via, and a conductive layer (for example, metal) is deposited over the dielectric. The bottom portion of the conductive layer in each via will form the back-side contact pad.

After the integrated circuit has been formed, the wafer is etched from the back side until the back-side contact pad is exposed. The etch etches the wafer substrate faster than it etches the dielectric separating the substrate from the pad. Therefore, the wafer substrate is receded relative to the dielectric so that the dielectric protrudes down relative to the substrate around each back-side contact pad. Thus the dielectric insulates the back-side contact pads from the substrate.

In some embodiments, the wafer is held by a non-contact wafer holder during the back-side etch. The face side of the wafer does not physically contact the holder. Therefore, there is no need to cover the face side with any protective layer to protect the wafer during the etch. Further, the holder protects the face side circuitry from the etch.

The wafer is diced into dice before or after the back-side etch.

In some embodiments, the back-side contact pads are used for vertical integration.

In some embodiments, the dice are not used for vertical integration. The dice are thinned to reduce their vertical dimension.

Other embodiments and variations are within the scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1-7, 8A and 8B are cross section illustrations of a semiconductor wafer in the process of fabrication of a back-side contact pad.

Figs. 9 and 10 show three dice having back-side contact pads of Fig. 8A; the dice are being connected together in a vertical integrated circuit.

Figs. 11-13 are cross-section illustrations of a semiconductor wafer in the process of creating a back-side contact pad.

Figs. 14 and 15 each show three dice connected in a vertical integrated circuit.

Fig. 16 illustrates the process and apparatus for thinning a semiconductor wafer by a back-side etch.

Figs. 17 and 18 illustrate thinning of individual dice.

DESCRIPTION OF PREFERRED EMBODIMENTS

Fig. 1 shows a wafer 104 a portion of which will provide a die having an integrated circuit with back-side contact pads. The back-side contact pads are suitable for connecting the die to an underlying die to create a "vertical integrated circuit". The two dice will be stacked on top of each other, reducing the lateral area taken by the circuit.

Wafer 104 includes silicon substrate 110. In some embodiments, the wafer has been processed to form

transistors, capacitors, resistors, conductive lines, and/or other circuit elements, or portions of circuit elements, in, above and/or below substrate 110. In other embodiments, no portions of any circuit elements have been formed. The wafer thickness is greater than the thickness of the die to be manufactured. In some embodiments, wafer 104 is 600-750 μm thick (dimension W is 600-750 μm). When the integrated circuit fabrication will be completed, the wafer will be thinned by an etch of the wafer back side 104B. The final thickness of the die will be 100-350 μm or less in some embodiments. Other thicknesses are achieved in other embodiments. Providing a greater wafer thickness at the beginning of fabrication makes the wafer stronger and thus increases the manufacturing yield.

Figs. 1-3 show an etch of silicon substrate 110 on the wafer face side to form vias in which the back-side contact pads will be fabricated. As shown in Fig. 1, an aluminum layer 120 is deposited on silicon 110. In some embodiments, the aluminum layer is 0.8-1.2 μm thick, 1 μm thick in some embodiments. Other thicknesses are used in other embodiments. Photoresist (not shown) is deposited and patterned. The aluminum 120 is etched to form an opening 124 exposing the silicon 110. In some embodiments, aluminum 120 is etched by an acid dip. In other embodiments, aluminum 120 is etched by a Cl-based vacuum plasma etch described in "VLSI Electronic Microstructure Science", the volume "Plasma Processing for VLSI" (edited by Norman G. Einspruch, Academic Press, Inc. 1984), hereby

incorporated herein by reference. Other aluminum etches are used in other embodiments.

The width of opening 124 is shown as A. In some embodiments, opening 124 is round of a diameter A. In other embodiments, the opening is a square having a side A. Other opening shapes are used in other embodiments. The center of the opening is located directly above the center of the corresponding back-side contact. The opening dimensions are not greater than the dimensions of the back-side contact pad to be formed under the opening.

Other openings similar to opening 124 are formed simultaneously at the location of each back-side contact pad. Different openings may have different shapes and dimensions in the same wafer.

The photoresist is stripped, and silicon 110 is etched with aluminum 120 as a mask (Fig. 2). In some embodiments, the silicon etch is an isotropic vacuum plasma etch described in the aforementioned volume "Plasma Processing for VLSI". Other known etches are used in other embodiments. The etch forms vias 130 of a depth B at the location of each back-side contact pad. Only one via 130 is shown in Figs. 2 and 3. The via depth B is at least as large as the final thickness of the die to be manufactured. In some embodiments, the bottom side of via 130 has the same shape and dimensions as the corresponding opening 124 in aluminum 120. The via widens as it goes up. As shown in Fig. 3, in some isotropic etch embodiments the dimensions of the top of via 130 are larger by 2B than the respective

dimensions of the bottom of the via. In other embodiments, the top dimension is A+2C, where $C \geq 0$, e.g. $0 \leq C \leq B$. If the etch is a perfectly anisotropic vertical etch (e.g. the horizontal etch rate is zero; this holds true for some known reactive ion etches), then $C = 0$.

Aluminum 120 is removed by an acid dip or another method known in the art (Fig. 3).

In some embodiments, the mask used in the etch of vias 130 is made of a photoresist; aluminum is not used for the mask. However, in some embodiments in which the via depth B exceeds 20 μm, the mask is formed from aluminum or another material sufficiently resistant to the silicon etch of vias 130.

A dielectric layer 140 (Fig. 4) is deposited over the wafer. In some embodiments, layer 140 is undoped silicon dioxide and/or BPSG, 1-2 μm thick, e.g. 1 μm thick. Other materials or thicknesses are used in other embodiments. In Fig. 4, layer 140 is BPSG formed by chemical vapor deposition at the atmospheric pressure. The distance between the top of silicon 110 and the bottom of vias 130 remains equal to B. Other deposition techniques, including thermal oxidation, are used in other embodiments.

A conductive layer 150 (Fig. 5) is deposited over dielectric 140. In some embodiments, layer 150 is a 0.8-1.2 μm (e.g. 1 μm) layer of aluminum, gold, or nickel; these metals can be deposited by vacuum sputtering. In other embodiments, layer 150 is some other metal or alloy used in VLSI for contact pads, for

example, aluminum doped with silicon or copper or both. The thickness of layer 150 in one Al/Si/Cu embodiment is 0.8-1.2 μm. The bottom portions 150C of layer 150 in vias 130 will provide the back-side contact pads.

The bottom portions 150C in vias 130 have about the same dimensions (such as A) as the respective openings 124 (Fig. 1).

A silicon dioxide glass layer 160 (Fig. 6) is deposited from TEOS and is spun on the wafer to fill the vias 130. Oxide 160 has a planar top surface. In some embodiments, no voids are left in the vias. Excess oxide 160 is etched off the wafer by a blanket etch so that the oxide remains in vias 130 but not outside the vias and the top surface of the wafer is planar.

Other materials and processes are used to fill vias 130 in other embodiments.

Conductive layer 150 is patterned by standard photolithographic techniques to form conductive lines (not shown) connecting the back-side contact pads 150C in vias 130 to integrated circuit elements (formation of these elements may not yet be completed at this point).

In some embodiments, layer 150 is patterned at the stage of Fig. 5 before the deposition of oxide 160 rather than after the deposition of oxide 160. The photoresist mask (not shown) used to pattern metal 150 protects the metal inside vias 130. After the patterning, the mask is removed, and spin-on glass 160

is deposited from TEOS. Glass 160 is used to planarize the wafer.

Then steps are performed to complete fabrication of the integrated circuit, forming other circuit elements and, in particular, face side contact pads. In the embodiment of Fig. 7, these steps include:

1. Chemical vapor deposition of a dielectric layer 170 (silicon dioxide, undoped and/or BPSG, 1 μm thick). Layer 170 is patterned if needed for circuit fabrication.

2. Deposition of the last metal layer 180 (e.g. 0.8-1.2 μm of Al/Si) over dielectric 170. Metal 180 is patterned to provide face side contact pads. In the embodiment of Fig. 7, one such pad 180C overlies a back-side pad 150C.

3. Deposition of protective dielectric 190 (such as undoped silicon dioxide and/or BPSG, 1 μm thick) over layer 180.

4. Masked etch of dielectric 190 to expose the underlying contact pads in metal 180.

Then the wafer 104 back side is etched by an atmospheric pressure plasma etch described in O. Siniaguine, "Plasma Jet Etching at Atmospheric Pressure for Semiconductor Production", 1996 1st International Symposium on Plasma Process-Induced Damage, May 13-14, 1996, California, U.S.A., pages 151-153 hereby incorporated herein by reference. A suitable etcher is PaceJet II (Trademark) available from IPEC/Precision, Inc. of Bethel, Connecticut and described in the Appendix hereinbelow. See also "PACEJET II - The

Revolutionary, Enabling Technology for Material Removal" (IPEC/Precision, 1996) incorporated herein by reference. A suitable alternative etcher is the plasma etcher of type "PLASM-AZ-05" described in "Plasma Jet Etching. Technology and Equipment. Silicon Wafer Thinning & Isotropical Etching at Atmospheric Pressure" (Az Corporation, Geneva, Switzerland, SEMICON/EUROPA '95), April 1995. See also the following PCT publications incorporated herein by reference: WO 96/21943 published July 18, 1996; WO 92/12610 published July 23, 1992; WO 92/12273 published July 23, 1992. The plasma is a fluorine containing plasma maintained at the atmospheric pressure. The etch parameters are as follows: Ar (1 slm) + CF4 (3 slm) plasma in air ambient at atmospheric pressure. ("Slm" stands for standard liters per minute.) The DC power is 12 kW. The wafer temperature is about 300°C. The silicon etch rate is about 10 μm/min for an 8-inch wafer. Thus, a wafer can be etched from a 720 μm thickness down to 120 μm in 1 hour. Alternatively, 1.6 wafers per hour can be etched from 720 μm down to 360 μm. The etch is illustrated in Fig. 16 described below.

This etch etches BPSG 140 about 10 times slower than silicon.

The etch does not etch the aluminum, gold or nickel in layer 150.

The resulting structure is shown in Fig. 8A. When silicon dioxide 140 becomes exposed during the back-side etch, the etch etches silicon dioxide 140 about 8-10 times slower than silicon 110. Therefore, when the silicon dioxide is etched off the back-side contact pads 150C, the bottom portions 140A, 140B of the silicon dioxide around the metal 150 protrude down father than silicon 110. These protruding portions 140A, 140B help insulate the silicon substrate 110 from metal 150. In some embodiments in which the oxide 140 is 1 μm thick, 10 μm of silicon is etched during the time during which 1 μm of oxide 140 is etched off the back-side contact pads 150C. Thus, the vertical dimension V of protruding oxide portions 140A, 140B is 8-10 μm (at least 9 μm in some embodiments), which is sufficient to insulate the back-side contact pads 150C from the silicon substrate in some embodiments.

In some embodiments, oxide 140 is thicker, and the vertical dimension V of the protruding portions 140A, 140B left after exposing the contact pads 150C is larger.

In some embodiments, the plasma processing continues to grow a dielectric layer 192 (Fig. 8B) on the wafer backside. In particular, when the etch has been completed, the fluorine containing gas (for example, CF_4) is turned off in the plasma reactor. Oxygen (or water vapor), or nitrogen, or both oxygen and nitrogen (for example, air), are supplied with the plasma. The oxygen and/or nitrogen react to silicon

110 to form silicon oxide (SiO or SiO_2), silicon nitride SiN_x (for example, Si_3N_4), and/or oxy-nitride SiO_xN_y.

In some embodiments, dielectric 192 is 0.01-0.02 μm thick to provide reliable electrical isolation in a packaged vertical integrated circuit powered by supply voltages below 5V.

In some embodiments of Fig. 8B, insulator 192 is grown at a wafer temperature of 300-500°C. The concentration of oxygen and/or nitrogen is 20-80%. In some embodiments using oxygen without nitrogen, the processing time is about 10 minutes to grow silicon oxide of a 0.02 μm thickness. The thickness of layer 192 can be increased by using higher wafer temperature, higher oxygen and/or nitrogen concentration, or longer processing time.

In embodiments having the layer 192, metal 150 is chosen so as not to form a non-conductive layer on its bottom surface during the layer 192 fabrication. Thus, in some embodiments, metal 150 is gold, platinum, or some other metal that does not react with the species (oxygen or nitrogen) used to form layer 192. In other embodiments, metal 150 is titanium, or some other metal, that forms a conductive layer (for example, TiN) when the dielectric 192 is grown. In still other embodiments, metal 150 is a stack of metal layers such that the bottom layer of the stack does not form a non-conductive material on its surface. For example, in some embodiments, the bottom layer is gold, platinum or titanium, and an overlying layer is aluminum.

Steps of fabrication of the integrated circuit elements can be intermixed with the back-side contact pad fabrication steps of Figs. 1-7, 8A, 8B in any suitable manner.

Then wafer 104 is diced into dice. Figs. 9-10 show vertical interconnection of three dice 200.1, 200.2, 200.3 which have been obtained from wafers processed as in Figs. 1-7, 8A, and possibly 8B (layer 192 is not shown in Figs. 9-10 but is present in some embodiments). Different dice 200 may contain different integrated circuits and may be obtained from different wafers 104. Suffix ".i" (i = 1, 2, 3) in reference numerals in Figs. 9-10 indicates correspondence to the same numeral of Figs. 1-7, 8A, 8B in die 200.i. For example, 150C.3 denotes a back-side contact pad in die 200.3.

After the wafers are diced, a solder ball 210.i (Fig. 9) is placed by a robot over each face-side contact pad in metal 180.i. Solder 210 has a lower melting temperature than metal 150 or any other metal possibly present in the dice. In some embodiments, solder 210.i is made of tin, lead or their alloys. In some embodiments, the solder melting temperature is 120-180 degrees Celsius.

Some embodiments use conductive epoxy or conductive polymer instead of solder.

The dice are aligned so that each back-side contact pad 150C which is to be connected to an underlying die is positioned over the respective solder ball 210 in the underlying die. For example, contact

pad 150C.3 is positioned over solder ball 210.2. In some embodiments, other dice (not shown) overly die 200.3 and underlie die 200.1. The dice are pressed together and heated. The heating temperature is sufficient to melt or soften the solder 210. The heating temperature is 120 to 180 degrees C in some embodiments. The pressure is sufficient to create a good electrical contact between face-side pads in metal 180 and the overlying back-side pads 150C. The force applied to press the wafers together is 100-200 grams in some embodiments.

The dimensions of the solder 210 and the openings in dielectric 190 that expose the face-side contact pads in metal 180 are chosen so that the melted solder does not reach the lateral edges of the back-side contact pads 150C. For example, the melted solder 210.2 does not reach the edge 150C.E.3 of contact pad 150C.3. The melted solder in contact with the corresponding back-side contact pad 150C is held at the center of the back-side contact pad by the surface tension force acting at the interface between the solder and the pad. As a result, solder 210 does not contact the silicon 110 of the overlying wafer. The protruding portions 140A, 140B (Fig. 8A) increase the distance between the exposed metal 150 and the silicon 110. Since the solder adheres to the metal but not to the oxide 140, the protruding portions 140A, 140B help to prevent the solder 210 from contacting the silicon 110. In the embodiments using dielectric 192 (Fig.

8B), the dielectric 192 provides additional protection against silicon 110 contacting the solder.

Then the structure is cooled. The dice remain connected together in a vertical integrated circuit.

To strengthen the structure, the structure is placed in a vacuum chamber, and a dielectric adhesive 220 is introduced between the dice 200 by methods known in the art. The adhesive fills the spaces between the contacts formed by solder 210.

Fig. 10 shows the structure with back-side contact pads 150C seated on solder 210. In some embodiments, the width W10 of each of the openings in dielectric 190 that expose the face-side contact pads is 50 to 100 μm. In some embodiments, each opening is round, and the opening width is the opening diameter. In other embodiments, the opening is square, and its width is its side length. The width W11 of each back-side contact pad 150C is 30-50 μm. The width is the diameter or the side length, as described above for the openings in dielectric 190. The distance D10 between the bottom surfaces of silicon substrates 110 of adjacent dice is below 50 μm. The aspect ratio of each via 130 is below 2:1 in some embodiments, and is about 1:1 in some embodiments. The low aspect ratio increases the yield. The large width of openings in dielectric 190 and of contact pads 150C, and hence the large area of solder connections, improves heat dissipation when local heating occurs.

The multi-die structure is then encapsulated into a plastic or ceramic package, or some other package, using methods known in the art.

In Figs. 11-13, the material 160 filling the vias 130 is metal rather than silicon dioxide. In Fig. 11, the wafer has been processed as shown in Figs. 1-5. A metal ball 160 is placed by a robot into each via 130 using a method known in the art. Alternatively, metal 160 is deposited by electrodeposition. Before the electrodeposition process, the wafer face side is masked by a dielectric mask (not shown). The mask is made of photoresist in some embodiments. An opening is made in the mask in the area of each via 130. Then electrodeposition is performed to deposit metal 160 into the vias through the openings. The mask is then removed. Other methods to deposit metal 160 are used in other embodiments.

Metal 160 has a higher melting temperature than solder 210 (Fig. 9) that will be used to make contacts between the dice. However, metal 160 has a lower melting temperature than layer 150. Suitable metals include tin (melting temperature 232°C), zinc (melting temperature 420°C), and their alloys. In some embodiments that use aluminum for interconnects, the metal 160 melting temperature does not exceed 600°C (the aluminum melting temperature is 660°C).

In some embodiments, the volume of metal 160 in each via 130 is less than the volume of the via so that when the metal 160 melts, it will not overflow its via.

The wafer is heated to melt the metal 160 (Fig. 12) without melting the layer 150. In Fig. 12, the top surface of the metal filling 160 is coplanar with, or below, the top surface of metal 150 outside the via. In some embodiments, metal 160 overflows the vias and spreads over the top surface of the wafer outside the vias.

Then any other circuit elements can be formed over the via surface as shown in Fig. 13. In particular, in some embodiments, metal layer 150 is patterned to form conductive lines as described above for the embodiment of Fig. 6. When the metal 150 is etched, any overlaying metal 160 that may have overflowed the vias 130 is etched at the same time.

Dielectric 170 (e.g. BPSG), last metal 180 (e.g. Al/Si) providing the face-side contact pads, and dielectric 190 (e.g. BPSG; see Fig. 13) are deposited and photolithographically patterned similarly to the embodiment of Fig. 7. In some embodiments, metal 180 is aluminum deposit by vacuum sputtering or thermal evaporation. The wafer temperature during deposition does not exceed 250-300°C. The wafer temperature does not exceed the melting temperature of metal 160.

The wafer is thinned as described above in connection with Fig. 8A. In some embodiments, dielectric 192 is deposited as described above in connection with Fig. 8B. In other embodiments, dielectric 192 is omitted. Then fabrication proceeds as shown above in Figs. 9 and 10. All the processing steps of Figs. 8A, 8B, 9, 10, including melting or

softening the solder 210, are performed at temperatures below the melting temperature of metal 160.

Metal 160 increases the mechanical strength of the integrated circuit. Metal 160 also improves heat dissipation when local heating occurs.

In Fig. 14, fillings 160 are omitted. After fabrication of the structure of Fig. 5, dielectric 190 (BPSG in some embodiments) is deposited directly on conductive layer 150. Dielectric 190 is removed in vias 130 by a masked etch. The etch also removes dielectric 190 from other selected areas of metal 150, such as area 150F, to form face-side contact pads away from vias 130.

The wafers are diced into dice. Solder balls 210 of a diameter larger than the depth of vias 130 are placed in the vias. Solder is also placed over those face-side contact pads 150F which are to be connected to back-side contact pads 150C of overlying dice. Solder 210 in vias 130 is sufficiently thick so that when the solder is melted or softened, the top surface of the solder is at about the same height as the top surface of solder portions (not shown) over contacts 150F. The dice 200 are aligned, pressed together, and heated, as described above in connection with Figs. 9-10. The solder melts or softens and creates contacts between adjacent dice.

In some embodiments, layer 190 of each die except the top die contacts silicon substrate 110 or dielectric 192 (if present) of the adjacent overlying die. Adhesive is omitted in some embodiments since

friction between layers 190 and silicon 110 or dielectric 192 creates sufficient resistance to shearing forces.

The width W14 of each via 130 at the top is 90-150 μm in some embodiments. The width W11 of each back-side contact pad 150C is 30-50 μm. The distance D14 between similar points on the adjacent dice, for example, between bottom surfaces of substrates 110 of the adjacent dice, is 30-50 μm.

In Fig. 15, face-side contact pads do not overlie vias 130. Face-side contact pads 150F are made outside vias 130. Pads 150F are made from Al/Si layer 150 as described above in Fig. 14, or from another metal layer. Fillings 160 are omitted in some embodiments, but are present in other embodiments. Solder balls 210 are placed in openings in BPSG 190 over contact pads 150F. The dice are aligned to position the back-side contact pads 150C over corresponding face-side contact pads 150F. The dice are heated and pressed together as described above in connection with Figs. 9, 10 and 14. Solder 210 forms contacts between the contact pads. Adhesive (not shown) is introduced in spaces between the dice as described above in connection with Figs. 9 and 10. Dielectric 192 (Fig. 8B) is present in some embodiments of Fig. 15 but not in other embodiments.

In some embodiments, the die thickness T15 measured from the top surface of dielectric 190 to the bottom surface of back-side contact pads 150C is 25 μm. Other thicknesses are used in other embodiments.

Fig. 16 illustrates the back-side plasma processing that includes the etch exposing the contact pads 150C and (optionally) the deposition of dielectric 192. The processing is performed at atmospheric pressure in etcher PaceJet II available from IPEC/Precision, Inc. and mentioned above, or some other etcher described above in connection with Fig. 8A. During the etch and deposition, the wafer 104 is held in a non-contact wafer holder 1610. The wafer face side is oriented towards the holder 1610. Holder 1610 holds the wafer from the top without physically contacting the wafer. See also the USSR inventor certificate 732198 of inventors A.F. Andreev and R.A. Luus, published May 8, 1980, and incorporated herein by reference. Circular gas flow (vortex) 1614 between wafer holder 1610 and wafer 104 holds the wafer up close to the holder, but does not allow the wafer to contact the holder. Hence, a protective layer is not needed to protect circuitry 1618 on the wafer face side from physical contact with the holder or from being etched or otherwise damaged by plasma jet 1624. Plasma jet generator 1620 moves horizontally so that the plasma jet 1624 generated by the generator scans the wafer back side 104B.

Fig. 17-18 show an alternate atmospheric-pressure process suitable for thinning the wafer. Fig. 17 consists of Figs. 17A-17D. Fig. 17A illustrates the wafer 104 right before the thinning process. Circuitry 1618 has been fabricated on the wafer face side. In some embodiments, the wafer thickness is 600-720 μm.

Silicon is removed from the wafer back side by known methods (e.g. mechanical grinding) to reduce the wafer thickness to 150-350 μm. The resulting wafer is shown in Fig. 17B. The wafer is diced into chips 200 (Fig. 17C). The thickness of each chip is 150-350 μm. The chips are tested and sorted as known in the art. The chips are thinned further by fluorine-containing plasma at atmospheric pressure, and (optionally) dielectric 192 is deposited on the back side immediately after the etch as shown in Fig. 18. The etcher and the process of Fig. 18 are similar to those of Fig. 16, but in Fig. 18 the non-contact chip holder 1610 holds several individual chips (3 chips in Fig. 18) rather than a wafer. Each chip 200 is placed in an individual segment of holder 1610 and is held in place by gas flow 1614 similarly to Fig. 16. The plasma jet 1624 scans all the chips from the back side until the dielectric 140 at the via bottoms is removed and (optionally) dielectric 192 is deposited. No protective layer for circuitry 1618 is needed.

The atmospheric-pressure backside etch of the chips reduces the chip thickness to below 50 μm (Fig. 17D).

Chips 200 can be stack packaged as described above in connection with Figs. 10, 14, 15.

The two-stage process of Fig. 17 (e.g. mechanical grounding followed by plasma processing) reduces manufacturing costs in some embodiments. Indeed, depending on the manufacturing yield, the area of the wafer occupied by "bad" dice together with unused

regions may be considerable, for example, 50% of the wafer. If the wafer is diced before the thinning is completed as in the process of Fig. 17, and only "good" dice are thinned to completion and (optionally) provided with dielectric 192, time and resources are saved in thinning and deposition as compared to thinning the whole wafer and depositing dielectric 192 over the whole wafer. Further, a wafer of a 6-8 inch diameter, thinned down to 50 μm, is more fragile than a die having the same thickness but smaller lateral dimensions (below 1 inch in some embodiments). This is another reason why the manufacturing costs in some embodiments of Fig. 17 are lower.

In some embodiments, the processes of Figs. 16, 17 and 18 are used to thin wafers or dice that are not used in vertical integrated circuits. In such embodiments, the back side etches may or may not expose any conductive contacts. The processes of Figs. 16-18 follow fabrication of one or more circuit elements in or over the face side of each die or wafer. Therefore, the circuit element fabrication is performed when the wafer is thicker than its final thickness and, therefore, is mechanically stronger.

The embodiments described above illustrate but do not limit the invention. In particular, the invention is not limited by the number of dice in a vertical integrated circuit (the number of dice can be any number greater than one), or by any particular thicknesses, opening widths, or other dimensions. The

invention is not limited by any particular materials. Non-silicon wafers are used in some embodiments.

APPENDIX

PaceJet II Technology For Material Removal

The PaceJet II from IPEC/Precision provides a method for backside film removal and wafer thinning. PaceJet II is a non-contact material removal system that reduces wafer or device manufacturing costs by eliminating process steps. It also enables wafer thinning to levels beyond the limitations of backside grinders.

PaceJet II employs an atmospheric pressure variant of IPEC's Plasma Assisted Chemical Etching, or PACE, technology. This method produces high etch rates without damaging the wafer substrate or front-side devices.

PaceJet II combines PACE technology with a non-contact wafer holding technique to provide significant advantages over conventional grinding and wet chemical etching.

FEATURES AND BENEFITS

Feature	Benefit
High-rate form of PACE	Increases throughput; produces smooth, uncontaminated, undamaged wafer surfaces
Five-wafer carousel processing	increases throughput
Planetary wafer motion	Provides uniform axi-symmetric etch removal
Ambient pressure operation	No vacuum - reduces complexity and cost
Non-contact wafer holder	For backside processing, eliminates contact with device side of wafer
Nitrogen "veil"	Holds wafer without surface contact; eliminates need to protect device side of wafer with resist/tape
Low-energy plasma	Eliminates risk of charge build-up on device side of wafer
Small footprint (1.3 m^2 or 13.9 ft^2)	Minimal cleanroom or chase area required

APPLICATIONS

Process	Process Steps Replaced or Reduced by PaceJet II	Benefits
Backside Film Removal	**Replaced:** (a) Grinding, wet etching or vacuum plasma (b) Resist coat for front surface protection (c) Resist strip(s)	Eliminates grinding damage, e.g., μcracks in Si Repeatability Reduces process steps and equipment No wet chemical handling
Backside Wafer Thinning	**Replaced:** (a) Resist coat (b) Wet etch (c) Resist strip(s)	Eliminates grinding/lapping thinness limitations Removes disordered layer without need for device-side protection Chip packaging, speed, and heat dissipation
Wafering	**Replaced:** (a) Lapping or grinding (b) Chemical etch **Reduced:** (a) # of polish steps (3) (b) # of cleans (3)	Lower cost/wafer Higher wafering yield Reduced capital
Bonded SOI Wafer Thinning	**Replaced:** (a) Fine grind (b) Polish & clean (optional) **Reduced:** # of inspections	Lower cost/bonded wafer Higher yield Reduced capital Improved SOI wafer quality

PERFORMANCE

Wafer Processing Throughput - Dependent on Wafer Size & Material Removal:

	Wafers per hour	
	150-mm	200-mm
400 nm Si_3N_4	180	144
20 µm Silicon	45	27

Surface Microroughness - Dependent on Si Removal Depth:

	Silicon Removal Depth (µm)		
	200	100	10
% Improvement in Initial µRoughness	86%	65%	10%
Example: initial roughness 100 nm, final =	14 nm	35 nm	90 nm

Added Material Removal Non-Uniformity - Independent of Si removal depth and wafer size: < 0.5 µm.

Cassette to Cassette, Fully Automated Operation.

System Footprint: Approximately 84 cm (W) X 156 cm (D)

CLAIMS

1. A method for fabricating an integrated circuit, the method comprising:

providing a body having one or more openings in a first side;

fabricating a first dielectric and a conductor in each of the one or more openings with the conductor in each of the openings being separated from the body by the first dielectric;

removing material from a second side of the body to expose the conductor in each of the openings wherein the removing of the material comprises a process in which the removal rate of the first dielectric is lower than the removal rate of material of the body.

2. The method of Claim 1 wherein in said process the removal rate of the first dielectric is about 10 times lower than the removal rate of the material of the body.

3. The method of Claim 1 wherein in said process the removal rate of the first dielectric is higher than the removal rate of the conductor.

4. The method of Claim 1 wherein the removal of the material from the second side of the body is followed by forming a second dielectric on the second side of the body but not on the conductor exposed on the second side.

5. The method of Claim 1 wherein removing material from the second side comprises plasma etching of the second side of the body at about an atmospheric pressure as the body is held in a non-contact holder.

6. The method of Claim 1 further comprising dicing the body before the removal of the material from the second side is completed, and

removing material from the second side comprises removing material from individual dice.

7. The method of Claim 6 wherein removing material from the second side comprises:

removing material from the second side before the body is diced; and

removing material from individual dice after the body is diced.

8. The method of Claim 6 wherein removing material from individual dice is preceded by testing of the dice of the body, and removing of the material from individual dice is performed only on a die or dice that have passed the test.

9. The method of Claim 1 wherein the body comprises semiconductor material.

10. The method of Claim 1 further comprising, after the removal of the material from the second side, connecting at least one integrated circuit of the body

to one or more other integrated circuits to form a vertical integrated circuit, with at least one of the exposed conductors contacting a contact pad of another integrated circuit.

11. An integrated circuit comprising:

a semiconductor body having one or more circuit elements formed in or over a first side of the body;

one or more conductive contacts protruding from a second side of the body, wherein at least one contact is connected by one or more conductive lines to one or more circuit elements formed in or over the first side; and

a dielectric separating each contact from the body, wherein the dielectric adjacent each contact protrudes out of the semiconductor material of the second side around each contact.

12. The integrated circuit of Claim 11 wherein the dielectric around each contact protrudes out of the semiconductor material of the second side by at least 8 μm measured in the direction perpendicular to the second side.

13. The integrated circuit of Claim 11 further comprising dielectric that covers the second side of the circuit but exposes the contact.

14. The integrated circuit of Claim 11 in combination with one or more other integrated circuits

such that at least one of the contacts contacts a conductive contact on another integrated circuit, the combination forming a vertical integrated circuit.

15. A method for fabricating an integrated circuit, the method comprising:

providing a body having one or more openings in a first side;

fabricating a first dielectric and a conductor in each of the one or more openings so that the conductor in each of the openings is separated from the body by the first dielectric;

removing material from a second side of the body to expose the conductor in each opening; and

forming a dielectric layer on the second side of the body by a process that does not form a dielectric layer on the one or more contacts.

16. The method of Claim 15 wherein forming the dielectric layer on the second side of the body comprises exposing the second side to a plasma containing a species that reacts with the material of the body to form the dielectric layer but which does not form a dielectric on the one or more contacts.

17. A method for manufacturing a vertical integrated circuit, the method comprising:

manufacturing a plurality of individual integrated circuits;

after the manufacture of the individual integrated circuits has been completed, and each individual integrated circuit has been manufactured to its final thickness, attaching the individual integrated circuits to each other to form a vertical integrated circuit.

18. The method of Claim 17 wherein manufacturing of the individual integrated circuits comprises a back side etch of at least one of the individual circuits as the circuit is held in a non-contact holder.

19. The method for integrated circuit fabrication, the method comprising:

fabricating a plurality of integrated circuits from a semiconductor wafer, wherein the wafer with the integrated circuits is thicker than the final thickness of each integrated circuit;

dicing the wafer into dice; and

thinning one or more dice obtained from the wafer as the one or more dice are held in a non-contact holder.

20. The method of Claim 19 wherein fabricating a plurality of integrated circuits comprises fabricating one or more circuit elements in or over a first side of the wafer, wherein each die has a first side which is part of the first side of the wafer; and

wherein during the thinning process, the first side of each of the one or more dice faces the non-contact holder which protects one or more of the

circuit elements fabricated in or over the first sides of the one or more dice from being etched.

21. The method of Claim 19 wherein the etching process comprises a fluorine containing plasma etch at atmospheric pressure.

22. The method of Claim 19 wherein the wafer comprises silicon.

23. The method of Claim 19 wherein the thinning of the one or more dice is preceded by testing of the integrated circuits, and the thinning is performed only on a die or dice that have passed the test.

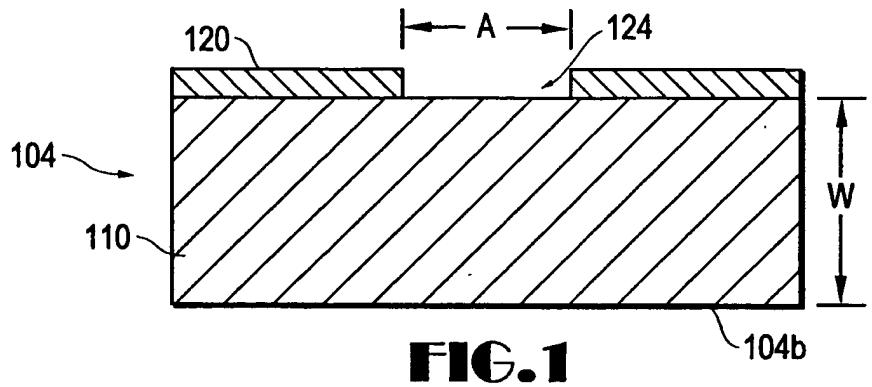


FIG.1

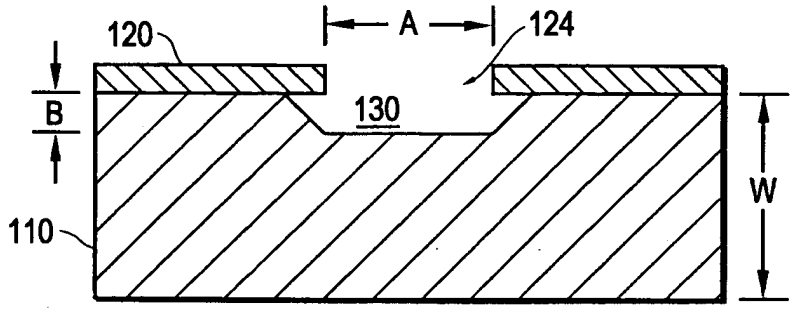


FIG.2

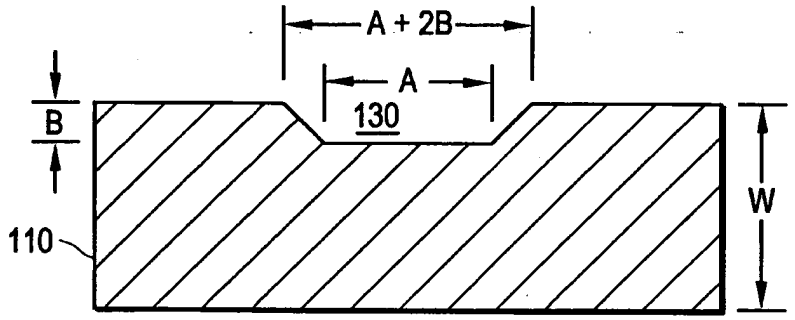


FIG.3

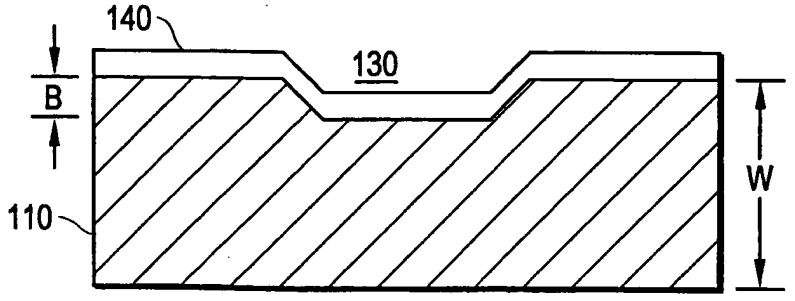


FIG.4

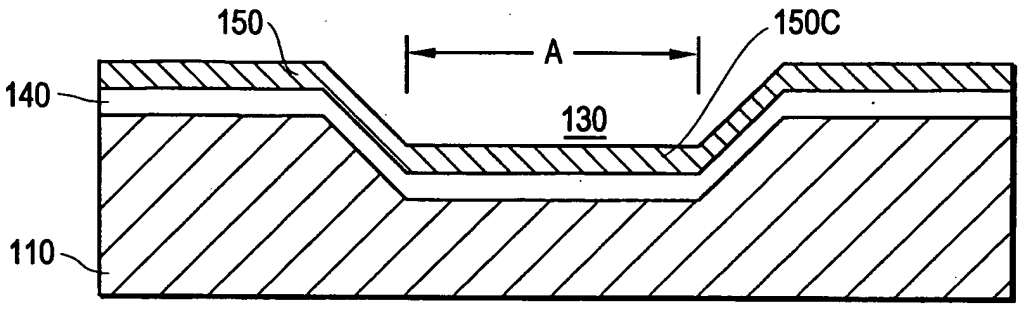


FIG.5

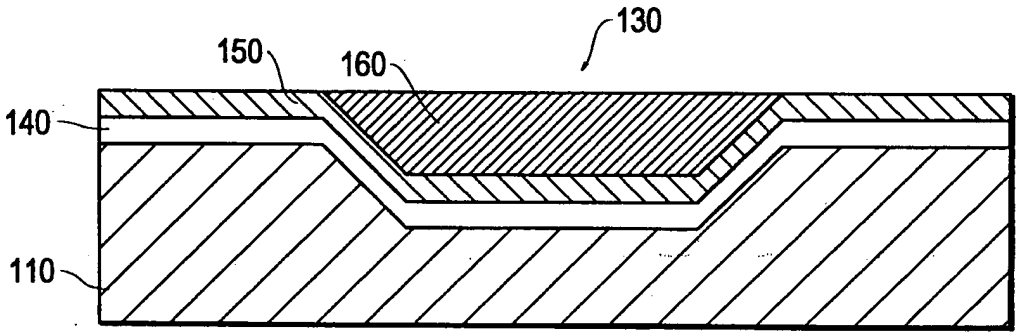


FIG.6

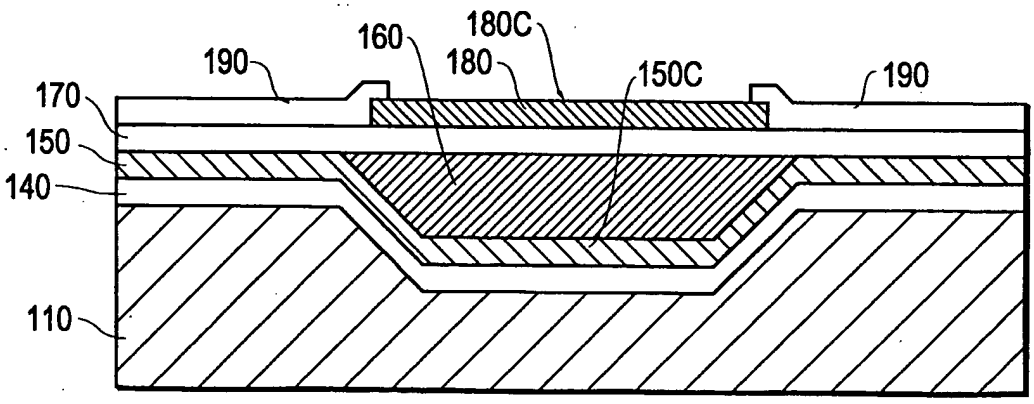
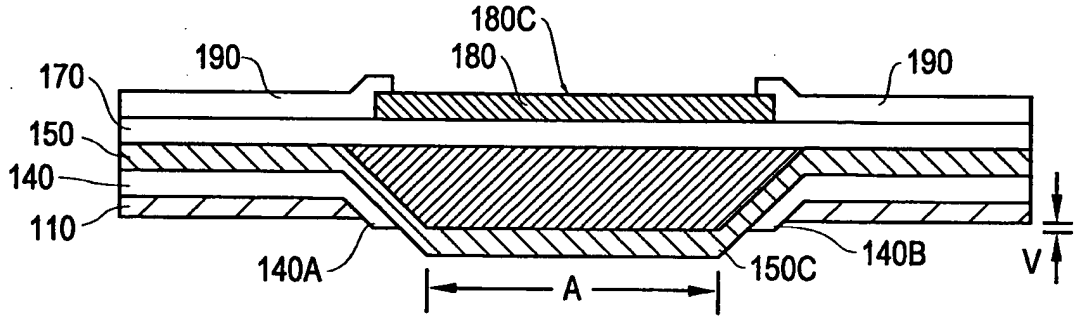


FIG.7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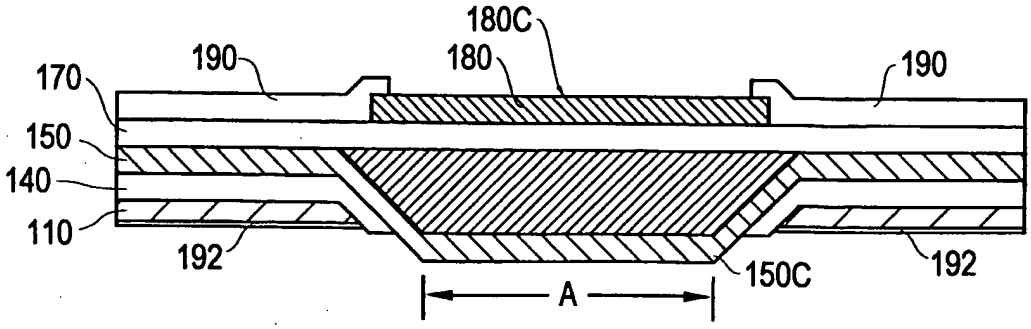
140B
V
A

FIG.8A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A

FIG.8B

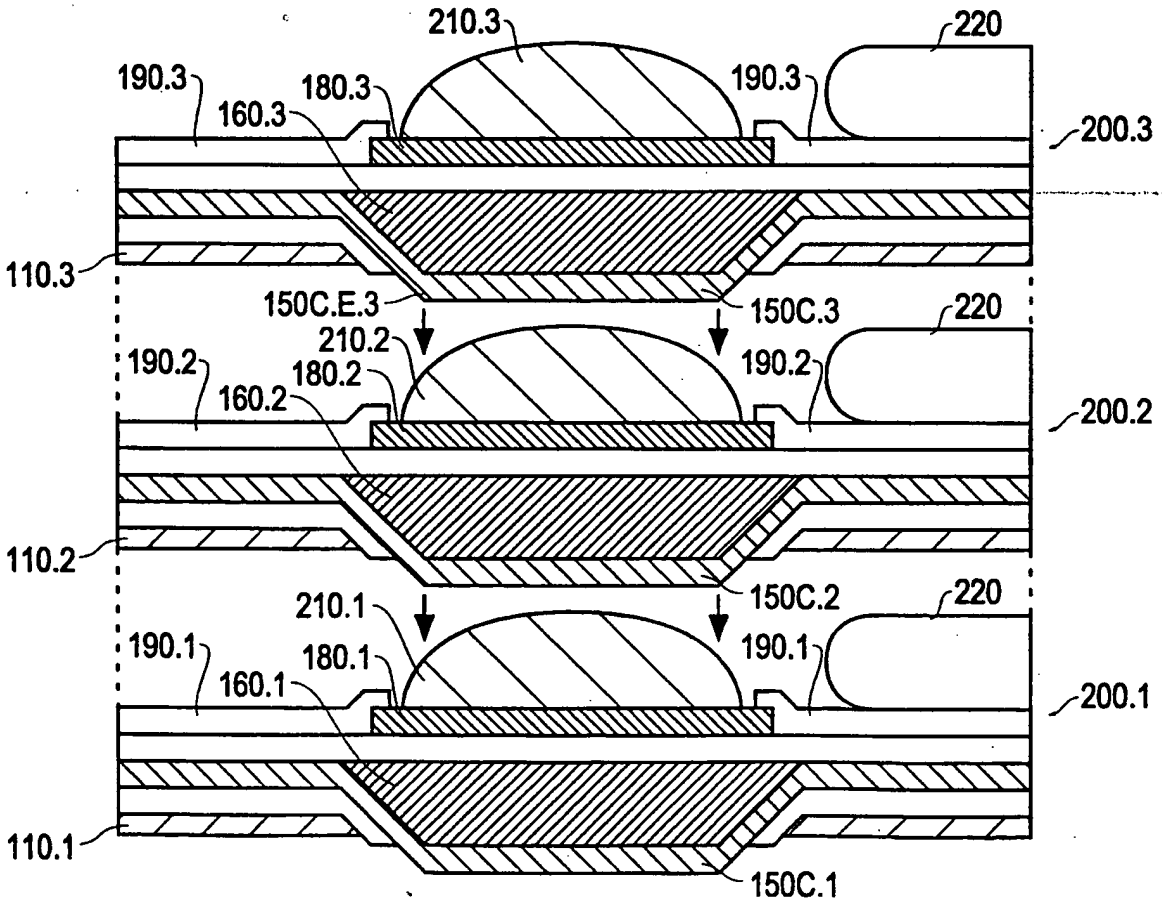
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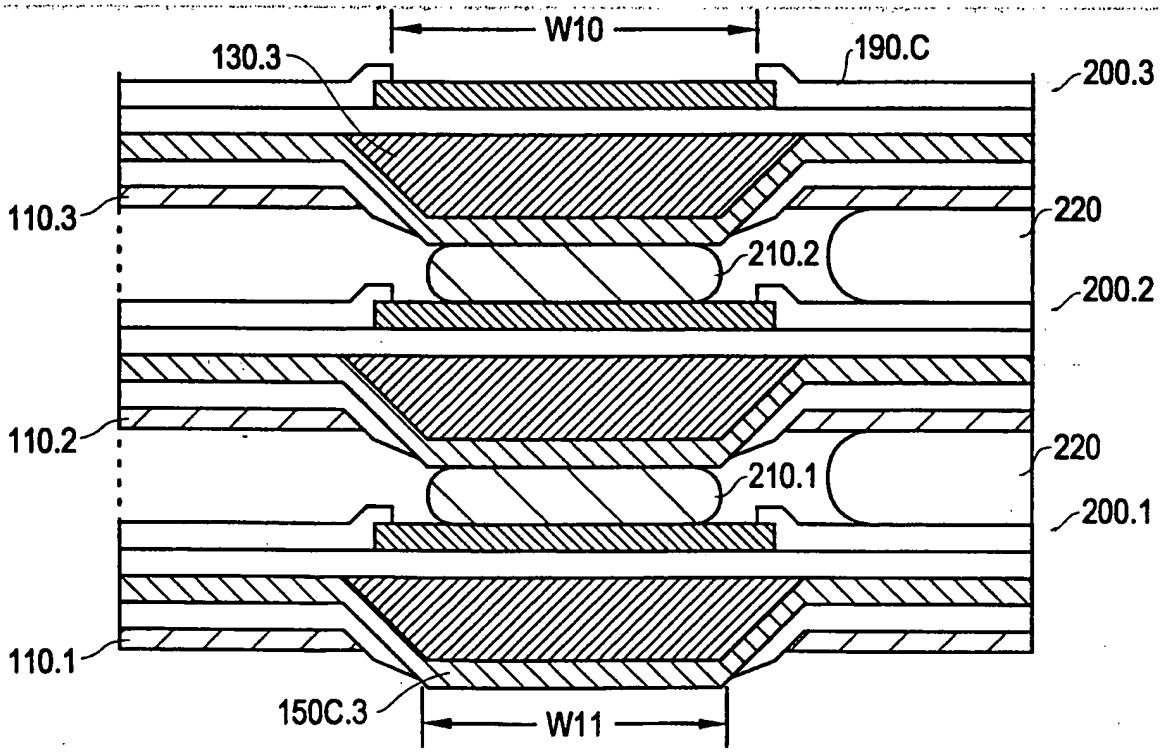
FIG.9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W11

FIG.10

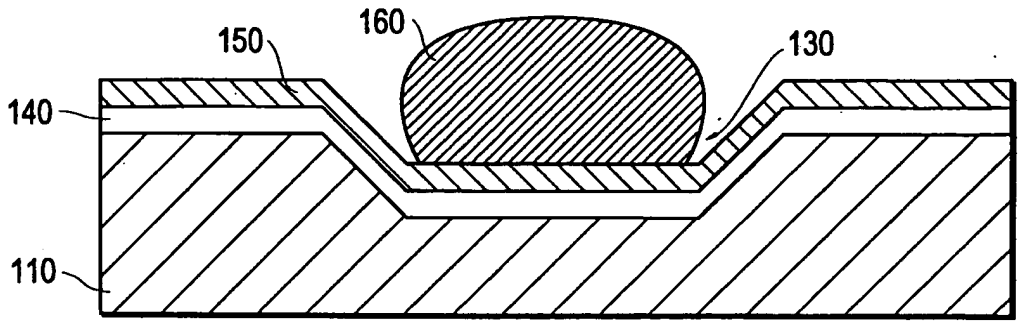


FIG.11

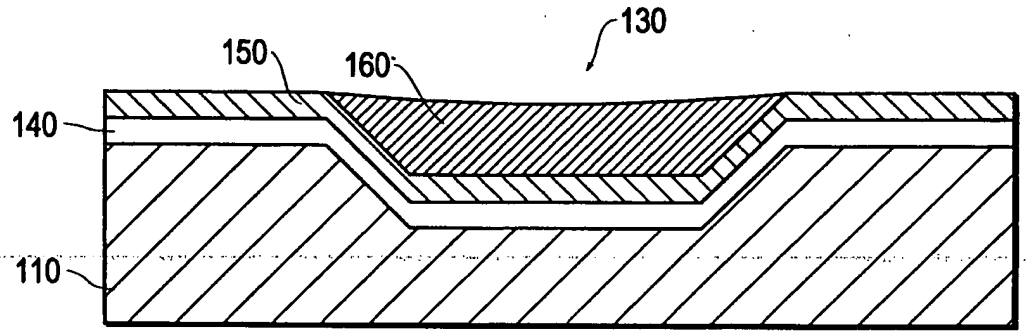


FIG.12

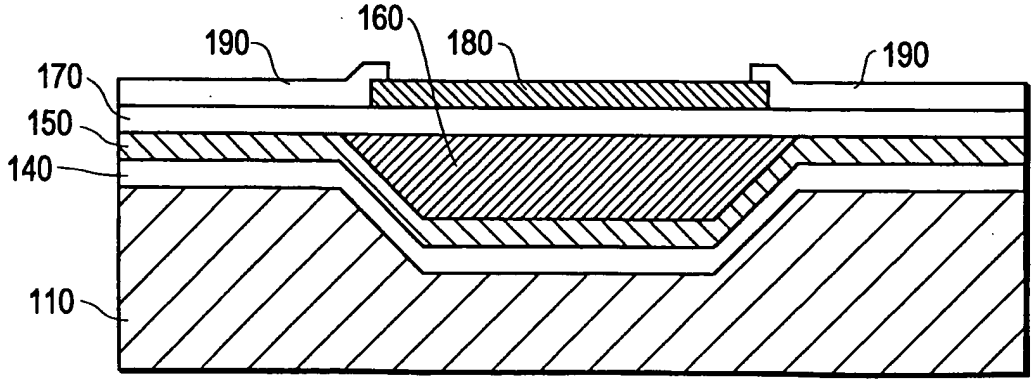
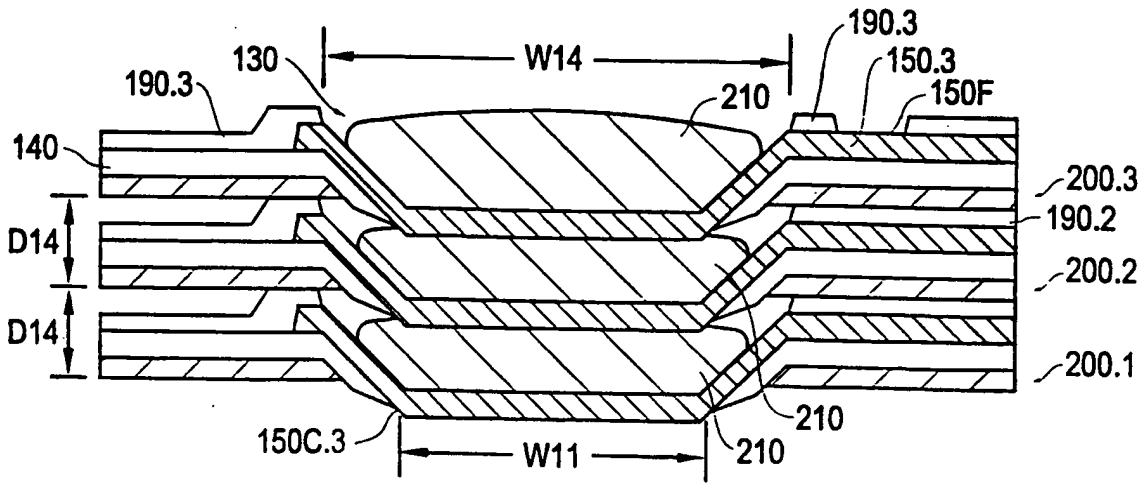


FIG.13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200.1
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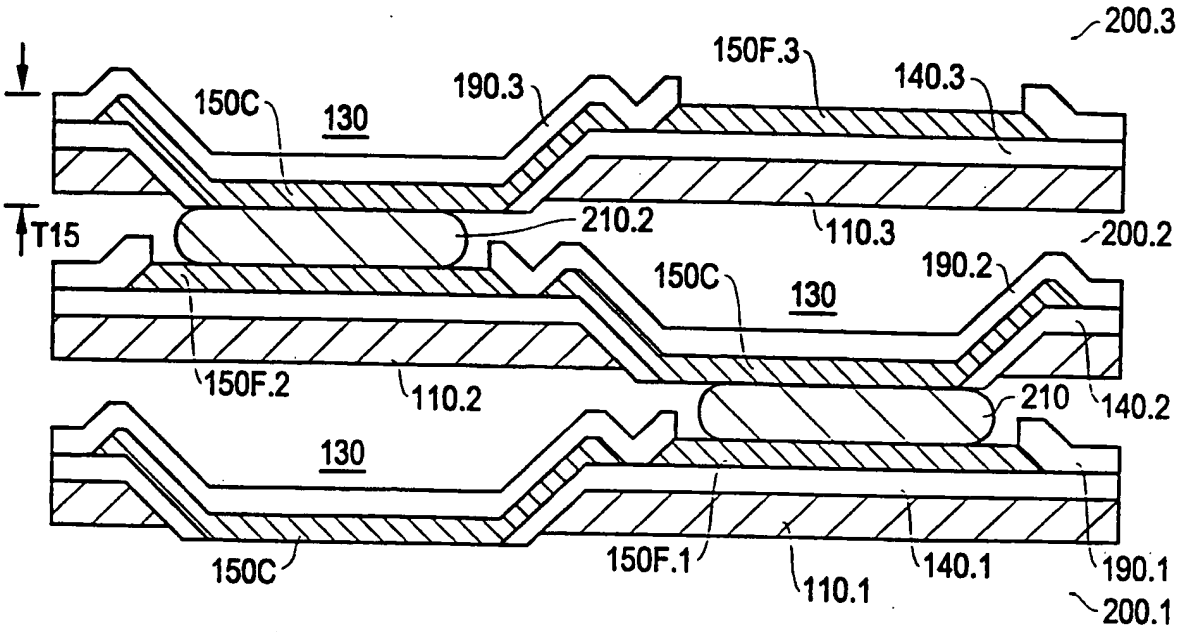
150C.3
W11
210

FIG.14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190.1
200.1

FIG.15

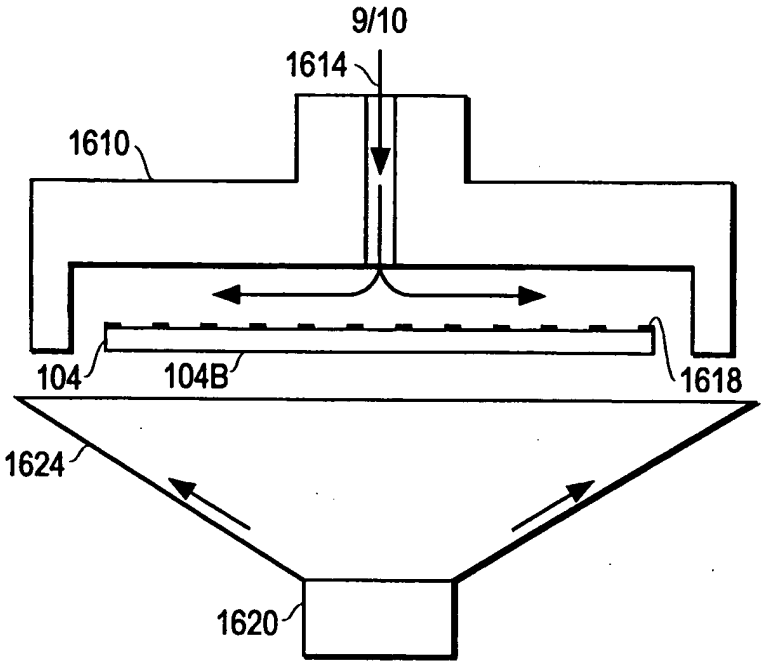

FIG.16

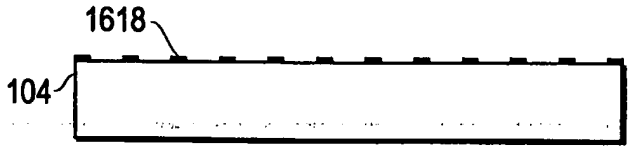

FIG.17A

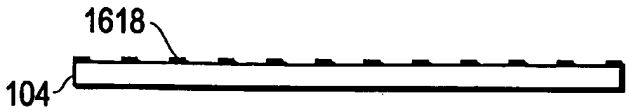

FIG.17B

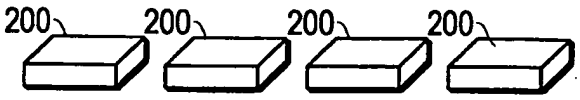

FIG.17C

FIG.17D

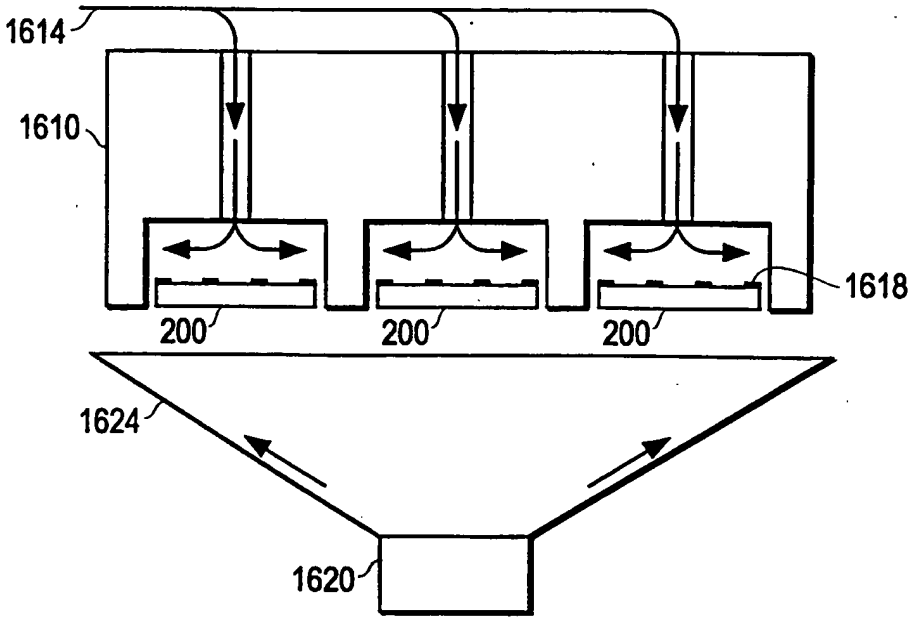

FIG.18

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/18979

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/44, 21/56, 21/60
US CL :438/108, 109, 459

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/108, 109, 113, 114, 455, 459

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,135,878 A (BARTUR) 04 August 1992 (04/08/92) col. 4, line 17, to col. 5, line 20.	1-23
Y	US 5,504,036 A (DEKKER et al) 02 April 1996 (02/04/96) col. 6, lines 5-56.	1-23
A	US 4,954,458 A (REID) 04 September 1990 (04/09/90) entire document.	1-23
A	US 5,270,261 A (BERTIN et al) 14 December 1993 (14/12/93) entire document.	1-23
A	US 5,472,914 A (MARTIN et al) 05 December 1995 (05/12/95) entire document.	1-23
A	US 4,141,135 A (HENRY et al) 27 February 1979 (27/02/79) entire document.	1-23

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
02 FEBRUARY 1998	0 4 MAR 1998
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer KEVIN M. PICARDAT Telephone No. (703) 308-0661

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